CH7517 DisplayPort to VGA Converter

FEATURES

- Compliant with DisplayPort specification version 1.2 and Embedded DisplayPort (eDP) specification version 1.3.
- Support 2 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s link rate
- Support analog RGB output for VGA with Triple 9-bit DAC up to 200MHz pixel rate. Sync signals can be provided in separated or composite manner. Support VESA and CEA timing standards up to 1920x1200@60Hz
- VGA output is compliant with VESA VSIS v1r2 specification
- Embedded MCU to handle the control logic
- Support device boot up by automatically loading firmware from on-chip flash Boot ROM
- Integrated EDID Buffer, and MCCS bypass supported
- Supports Enhanced Framing Mode
- Fast and full Link Training for embedded DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- 2 work modes: connect 27MHz crystal, inject 27MHz clock
- DAC connection detection supported
- DP input detection supported
- Support Auto Power Saving mode and low stand-by current
- Support Spread Spectrum Clocking (de-spreading) for EMI reduction
- DP AUX channel and IIC slave interface are available for firmware update and debug
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN package (5 x 5 mm)

APPLICATION

- Notebook/Ultrabook
- Tablet Device
- Handheld/Portable Device
- PC

GENERAL DESCRIPTION

Chrontel's CH7517 is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the VGA. This innovative DisplayPort receiver with an integrated VGA encoder is specially designed to target the notebook/ultrabook, tablet device and PC market segments. Through the CH7517's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to analog RGB video output.

The CH7517 is compliant with the DisplayPort specification version 1.2 and the Embedded DisplayPort Specification version 1.3. In the device's receiver block, which supports two DisplayPort Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8, and converted the input signal to VGA output up to 1920x1200@60Hz. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7517 is capable of instantly bring up the video display to the VGA monitor when the initialization process is completed between CH7517 and the graphic chip.

The DACs are based on current source architecture. And the VGA output meet VESA VSIS v1r2 clock jitter target. With sophisticated MCU and the Boot ROM embedded, CH7517 support auto-boot and EDID buffer. After the configuration by firmware, which is auto loaded from Boot ROM, CH7517 can support DP input detection, DAC connection detection and determine to enter into Power saving mode automatically.

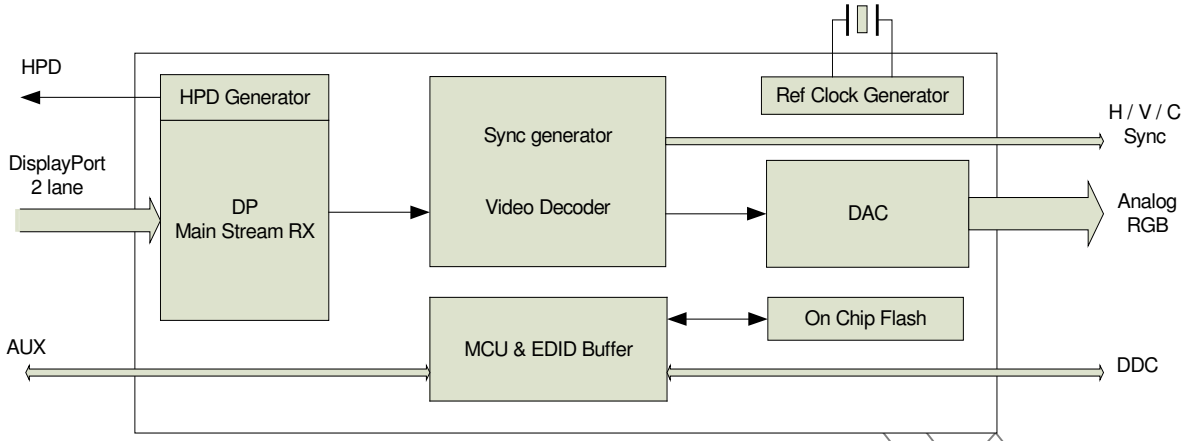

Figure 1: CH7517 Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

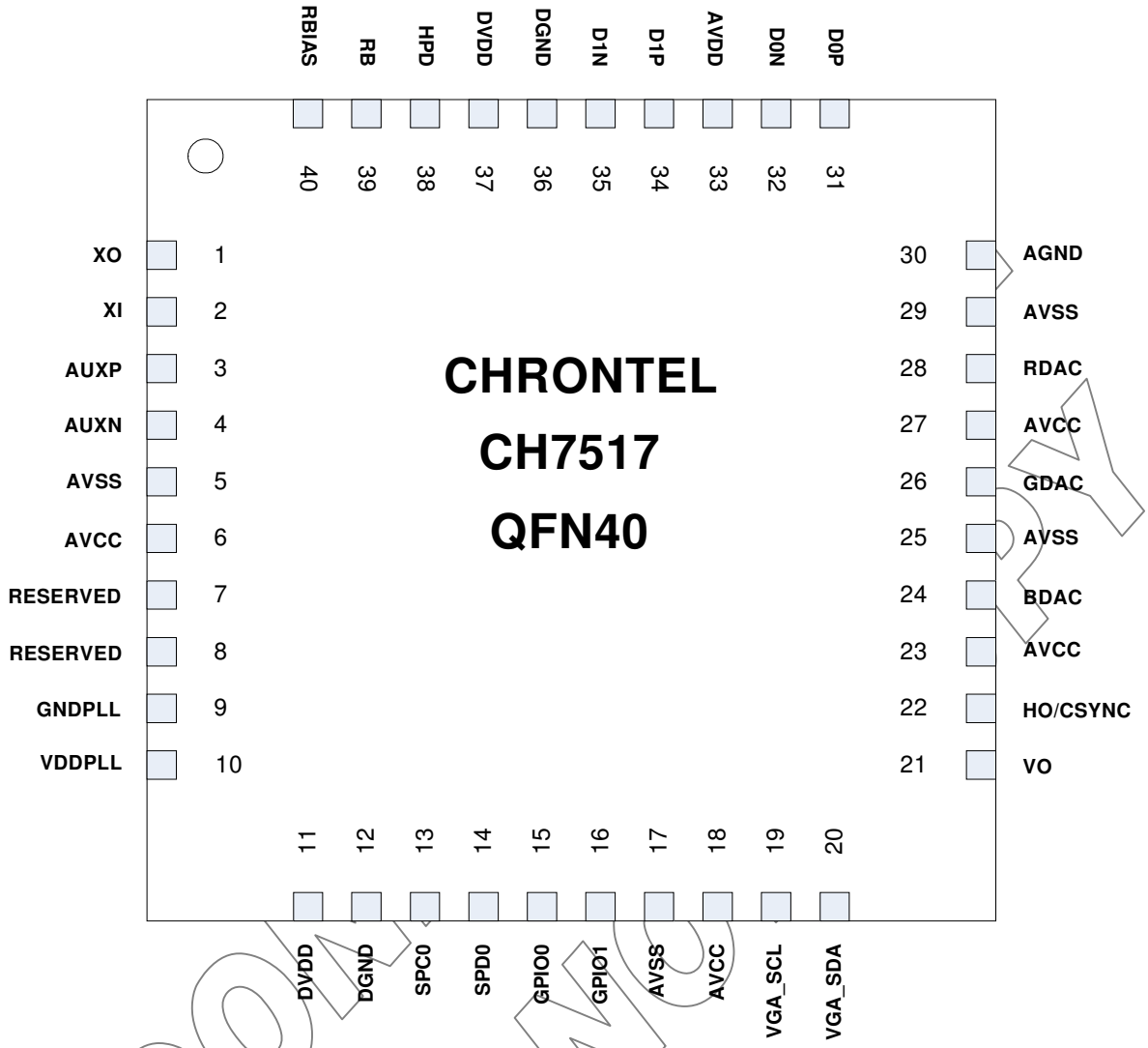

Figure 2: CH7517 40-pin QFN pin out

1.2 Pin Description

Table 1: Pin Name Descriptions

Pin #	Type	Symbol	Description
1	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open.
2	In	XI	**Crystal Input** A parallel resonance crystal should be attached between this pin and XO.
3,4	In/Out	AUXP/N	**DisplayPort AUX Port** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
7,8		RESERVED	**Reserved Pins**
13	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
14	In/out	SPD0	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
15,16	In/Out	GPIO[1:0]	**General Purpose Input/Output**
19	Out	VGA_SCL	**Serial Port Clock Output to VGA Receiver** The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level
20	In/Out	VGA_SDA	**Serial Port Data to VGA Receiver** The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level
21	Out	VO	**VGA VSYNC Output**
22	Out	HO/CSYNC	**VGA HSYNC/CSYNC Output** XOR Gate is default
24	Out	BDAC	**Blue Component Output**
26	Out	GDAC	**Green Component Output**
28	Out	RDAC	**Red Component Output**
31,32,34,35	In	D[1:0]P/N	**DP Rx Input Lane 1 and Lane 0**
38	Out	HPD	**DP Receiver Hot Plug Output**
39	In	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
40	In	RBIAS	**Current Set Resistor Input** This pin sets the DAC current. A 10KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces
6,18,23,27	Power	AVCC	**Analog Power Supply (3.3V)**
5,17,25,29, Pad	Power	AVSS	**Analog Power Ground**
9,	Power	GNDPLL	**PLL Power Ground**
10	Power	VDDPLL	**PLL Power Supply (1.2V)**
11,37	Power	DVDD	**Digital Power Supply (1.2V)**
12,36	Power	DGND	**Digital Ground**
30	Power	AGND	**Analog Power Ground**

33	Power	AVDD	**Analog Power supply (1.2v)**

2.0 PACKAGE DIMENSION

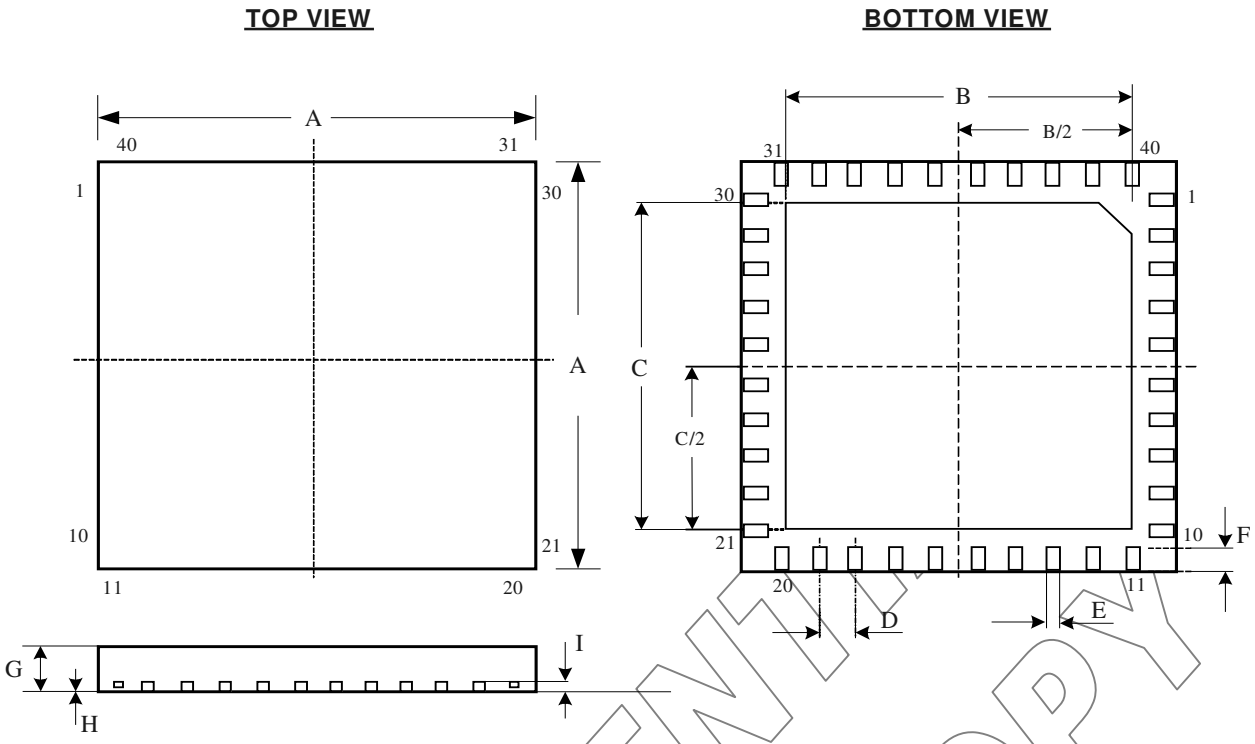

Figure 3: 40 Pin QFN Package

Table 2: Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.7	0	0.20
	MAX	5.10	3.75	3.75		0.25	0.55	0.8	0.05	0.203

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7517A-BF	40 QFN, Lead-free	Commercial : 0 to 70°C	490/Tray
CH7517A-BFI	40 QFN, Lead-free	Industrial : -40 to 85°C	490/Tray

Chrontel

Chrontel International Limited

129 Front Street, 5th floor,

Hamilton, Bermuda HM12

www.chrontel.com
E-mail: sales@chrontel.com